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APPLICATION NO. FILING DATE		FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/668,983 09/22/2003		Lin-Kai Bu	250807-1040	1768	
24504	7590 05/17/2006		EXAMINER		
	KAYDEN, HORSTE	SHAPIRO, LEONID			
STE 1750	RIA PARKWAY, NW	ART UNIT	PAPER NUMBER		
ATLANTA,	GA 30339-5948	2629			

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No. Appli		Applicant(s)	licant(s)					
		10/668,983		BU ET AL.						
Office Action Summary			Examiner		Art Unit					
		Leonid Shap	iro	2629						
	The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply									
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).										
Status										
1)☐ Resp	oonsive to communication(s) file	ed on 22 Sea	eptember 200	03.						
· — ·	• •		s action is non-final.							
3)		-	vance except for formal matters, prosecution as to the merits is							
close	closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.									
Disposition of	f Claims									
4)⊠ Clain	n(s) <u>1-12</u> is/are pending in the a	application.								
4a) Of the above claim(s) is/are withdrawn from consideration.										
5) Claim(s) is/are allowed.										
6)⊠ Claim(s) <u>1-12</u> is/are rejected.										
7)∐ Clain	n(s) is/are objected to.									
8)∏ Clain	n(s) are subject to restric	ction and/or	election req	uirement.						
Application Pa	apers									
9)∐ The s	pecification is objected to by th	e Examiner.	•							
10)⊠ The drawing(s) filed on <u>22 Se<i>ptember</i> 2003</u> is/are: a)⊠ accepted or b)⊡ objected to by the Examiner.										
Appli	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).									
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).										
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.										
Priority under	35 U.S.C. § 119									
<ul> <li>12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).</li> <li>a) All b) Some * c) None of:</li> <li>1. Certified copies of the priority documents have been received.</li> <li>2. Certified copies of the priority documents have been received in Application No</li> </ul>										
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).										
* See the attached detailed Office action for a list of the certified copies not received.										
Attachment(s)										
1) Notice of References Cited (PTO-892)  4) Interview Summary (PTO-413)  2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  Paper No(s)/Mail Date										
3) X Information	Disclosure Statement(s) (PTO-1449 or /Mail Date		5) Notice of Informal Patent Application (PTO-152) 6) Other:			O-152)				

## Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 1. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA (Admitted Prior Art) in view of Maki (Pub.: US 2003/0146909 A1) and Ahn et al. (US Patent No. 7,015,889 B2).

As to claim 1, APA teaches a data driver for driving multiple data lines on an LCD panel according to multiple channels of pixel data (See Fig. 2, paragraph 0004), the data driver comprising:

a digital buffer for receiving and storing the pixel data at several times and selectively outputting a channel of the pixel data at a time (See Fig. 2, item 214, paragraph 0005);

an output buffer for receiving the analog pixel data output from the analog buffer so as to drive the data lines (See Fig. 2, item 218, paragraph 0007).

APA does not disclose a DAC (digital-to-analog converter) for receiving the pixel data output from the digital buffer at several times, converting the pixel data into multiple channels of analog pixel data and outputting the analog pixel data at several times;

an analog buffer for receiving the analog pixel data output from the DAC at several times and for outputting the analog pixel data at a time.

Maki teaches DAC for receiving the pixel data output from the digital buffer at several times, converting the pixel data into multiple channels of analog pixel data and outputting the analog pixel data at several times (See Fig. 2, item 20, paragraphs 0029-0032).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teachings of Maki into APA system in order to reduce chip area by reducing the number of DACs (See paragraph 0008 in the Maki reference).

APA and Maki do not disclose an analog buffer for receiving the analog pixel data output from the DAC at several times and for outputting the analog pixel data at a time.

Ahn et al. teaches an analog buffer for receiving the analog pixel data output from the DAC at several times and for outputting the analog pixel data at a time (See Fig. 2, items 203-205, from Col. 1, Line 65 to Col. 2, Line 34).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teachings of Ahn et al. into Maki and APA system in order to reduce output deviations (See Col. 1, Lines 39-40 in the Ahn et al. reference).

As to claim 2, APA teaches a shift register for commanding the digital buffer to receive the pixel data (See Fig.2, items 212, 214, C).

As to claims 3-4, APA teaches the digital buffer includes a first line buffer and a second line buffer; the first line buffer receives and stores the pixel data at several times', when the first line buffer finishes its receiving operations, the first line buffer parallely transfers all the pixel data stored therein to the second line buffer; and the second line buffer outputs a channel of the pixel data to the DAC at a time (See Fig. 2, items 212, 214, C, paragraphs 0005-0006).

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As to claims 5-6, Ahn et al. teaches he analog buffer comprises multiple analog buffer units and the analog buffer units receive the analog pixel data output from the DAC at several times and analog buffer control circuit for commanding the analog buffer to receive the analog pixel data output from the DAC and to store the analog pixel data in the analog buffer units at several times, and for commanding the analog buffer to parallely output the analog pixel data to the output buffer after the analog buffer finishes its receiving operations (See Fig. 2, items 203-205, from Col. 1, Line 65 to Col. 2, Line 34).

2. Claims 7-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama et al. (JP 11-167373) in view of Ahn et al. and APA.

As to claim 7, Koyama et al. teaches a data driver for driving multiple data lines on an LCD panel according to multiple channels of pixel data (See Drawing 2, paragraph 0037), the data driver comprising:

a digital buffer for receiving and storing the pixel data at several times and selectively outputting N channels of the pixel data at a time, wherein N is a positive integer greater than 1 and smaller than the number of the data lines (See Drawing 2, items 203-204, paragraph 0038);

N sets of DACS (digital-to-analog converters) for receiving the pixel data output from the digital buffer, simultaneously converting N channels of the pixel data into N channel of analog pixel data, and outputting the analog pixel data (See Drawings 2, 14, item 208, paragraph 0039).

Koyama et al. does not disclose an analog buffer for receiving the analog pixel data output from the DACS at several times and outputting the analog pixel data at a time; and an

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output buffer for receiving the analog pixel data output from the analog buffer so as to drive the data lines.

Ahn et al. teaches an analog buffer for receiving the analog pixel data output from the DAC at several times and for outputting the analog pixel data at a time (See Fig. 2, items 203-205, from Col. 1, Line 65 to Col. 2, Line 34).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teachings of Ahn et al. into Koyama et al. system in order to reduce output deviations (See Col. 1, Lines 39-40 in the Ahn et al. reference).

Koyama et al. and Ahn et al. does not disclose an output buffer for receiving the analog pixel data output from the analog buffer so as to drive the data lines.

APA teaches an output buffer for receiving the analog pixel data output so as to drive the data lines (See Fig. 2, item 218).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teachings of APA into Ahn et al. and Koyama et al. system in order to enhance capability for driving the data lines (See paragraph 0007 in APA).

As to claim 8, Koyama et al. teaches the shift register for commanding the digital buffer to receive the pixel data (See Drawing 2, item 201).

As to claims 9-10, Koyama et al. teaches the digital buffer comprises a first line buffer and a second line buffer; the first line buffer receives and stores the pixel data at several times; when the first line buffer finishes its receiving operations, the first line buffer parallely transfers all the pixel data stored therein to the second line buffer; and

the second line buffer selectively outputs N channels of the pixel data to the DACS at a time (See Drawing 2, items 203-204, paragraphs 0037-0042).

As to claims 5-6, Ahn et al. teaches he analog buffer comprises multiple analog buffer units and the analog buffer units receive the analog pixel data output from the DAC at several times and analog buffer control circuit for commanding the analog buffer to receive the analog pixel data output from the DAC and to store the analog pixel data in the analog buffer units at several times, and for commanding the analog buffer to parallely output the analog pixel data to the output buffer after the analog buffer finishes its receiving operations (See Fig. 2, items 203-205, from Col. 1, Line 65 to Col. 2, Line 34).

## Telephone Inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LS 05.05.06

> RICHARD HJERPE SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2600